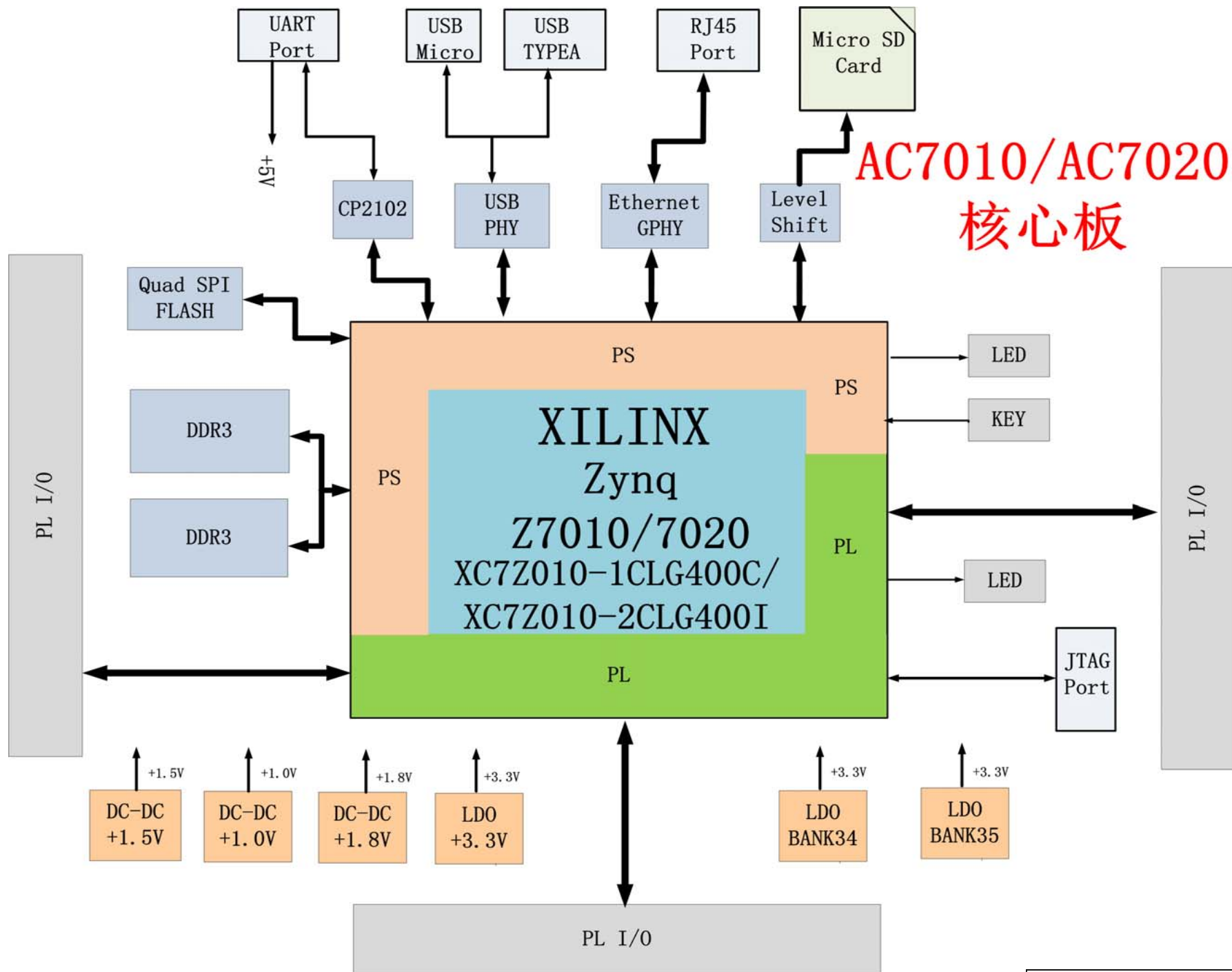


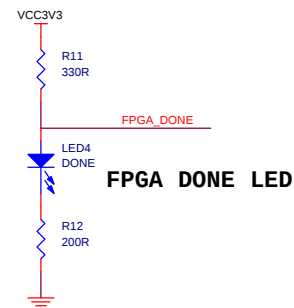
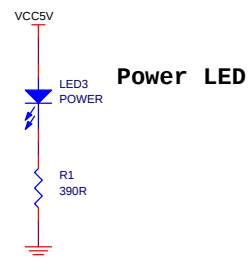
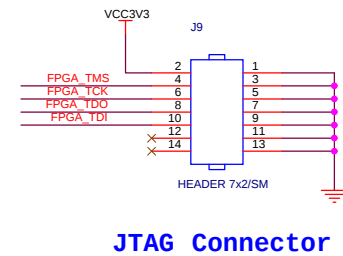
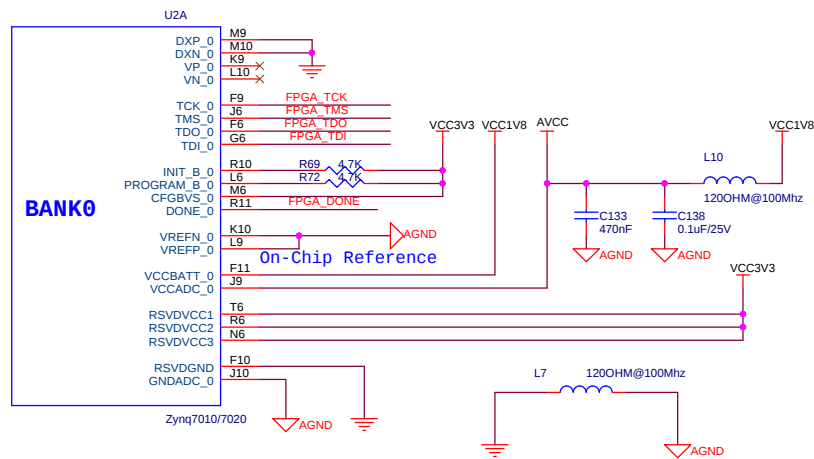
REV	Description	Date
V1.0	First Release	2017-1-12

AC7010/AC7020 Schematics

Page Number	Description
Page01	Cover Page
Page02	Block Diagram
Page03	Zynq-7000 JTAG & Bank0
Page04	Zynq-7000 MIO Config
Page05	Zynq-7000 Bank13-34-35
Page06	Zynq-7000 Bank502
Page07	Zynq-7000 Power
Page08	DDR3
Page09	GPHY
Page10	USB OTG
Page11	UART, SD
Page12	EXTEND IO
Page13	POWER



AC7010/AC7020 核心板



BOOT OPTION

PS_MIO8
QSPI_D0
QSPI_D1
QSPI_SCK
PS_MIO7

```

MIO[8] = 1  ---MIO bank501 voltage=1.8V
MIO[2] = 0  ---cascaded JTAG
MIO[3] = 0  ---JTAG/NAND/Quad-SPI/SD
MIO[6] = 0  ---PLL used
MIO[7] = 0  ---MIO bank0 voltage=3.3V
    
```

QSPI_D3
QSPI_D2
QSPI_SCK
QSPI_D0

Boot Mode	MIO[5] (QSPI_D3)	MIO[4] (QSPI_D2)
JTAG	0	0
NAND	0	1
QSPI - FLASH	1	0
SD Card	1	1

Boot Mode	MIO[5] (QSPI_D3)	MIO[4] (QSPI_D2)
JTAG	0	0
NAND	0	1
QSPI-FLASH	1	0
SD Card	1	1

U2B

BANK500

Zynq7010/7020

PS_MIO0_500
A7
PS_MIO1_500
B8
PS_MIO2_500
D6
PS_MIO3_500
B7
PS_MIO4_500
A6
PS_MIO5_500
A5
PS_MIO6_500
D8
PS_MIO7_500
D5
PS_MIO8_500
B5
PS_MIO9_500
E9
PS_MIO10_500
C6
PS_MIO11_500
D9
PS_MIO12_500
E8
PS_MIO13_500
C5
PS_MIO14_500
C8
PS_MIO15_500
C7
PS_POR_B_500
E7
PS_CLK_500

E5
A7
B8
D6
B7
A6
A5
D8
D5
B5
E9
C6
D9
E8
C5
C8
C7
E7

LED2
RED
R6
330R
R20
33R
PS_QSPI_CS
QSPI_D0
QSPI_D1
QSPI_D2
QSPI_D3
QSPI_SCK
PS_MIO7
PS_MIO8
PS_MIO9
PS_MIO10
PS_MIO11
PS_MIO12
PS_MIO13
PS_MIO14
PS_MIO15
PS_POR_B

QSPI_CS
QSPI_D0
QSPI_D1
QSPI_D2
QSPI_D3
QSPI_SCK
PS_MIO8
PS_MIO9
PS_MIO10
PS_MIO11
PS_MIO12
PS_MIO13
PS_MIO14
PS_MIO15
PS_POR_B

70
10
10
10
10
10
10
12
12
12
12
12
12
12
12
9

VCC3V3
33.333333Mhz
0.1uF/25V
C27
X2
3
4
1
2
GND
VDD
OE

R22
33R

VCC1V8

BANK501

PS_MIO_VREF_501

PS_MIO4_501

PS_MIO17_501

PS_MIO18_501

PS_MIO19_501

PS_MIO20_501

PS_MIO21_501

PS_MIO22_501

PS_MIO23_501

PS_MIO24_501

PS_MIO25_501

PS_MIO26_501

PS_MIO27_501

PS_MIO28_501

PS_MIO29_501

PS_MIO30_501

PS_MIO31_501

PS_MIO32_501

PS_MIO33_501

PS_MIO34_501

PS_MIO35_501

PS_MIO36_501

PS_MIO37_501

PS_MIO38_501

PS_MIO39_501

PS_MIO40_501

PS_MIO41_501

PS_MIO42_501

PS_MIO43_501

PS_MIO44_501

PS_MIO45_501

PS_MIO46_501

PS_MIO47_501

PS_MIO48_501

PS_MIO49_501

PS_MIO50_501

PS_MIO51_501

PS_MIO52_501

PS_MIO53_501

PS_SRST_B_501

B10

E11

A19 ETH TXCK

E14 ETH TXD0

B18 ETH TXD1

D10 ETH TXD2

A17 ETH TXD3

F14 ETH TXCTL

B17 ETH RXCK

D11 ETH RXD0

A16 ETH RXD1

F15 ETH RXD2

A15 ETH RXD3

D13 ETH RXCTL

C16 OTG DATA4

C13 OTG DIR

C15 OTG STP

E16 OTG NXT

A14 OTG DATA0

D15 OTG DATA1

A12 OTG DATA2

F12 OTG DATA3

A11 OTG CLK

A10 OTG DATA5

E13 OTG DATA6

C18 OTG DATA7

D14 R13_40 2R/1% SD OTG DATA7

C17 SLY CMD

E12 SD D0

A9 SD D1

F13 SD D2

B15 SD D3

D16 OTG RESETN

B14 SD CD

B12 UART TX

C12 UART RX

B9

C10 ETH MDC

C11 ETH MDIO

B10 PS SRST_B

ETH_TXCK

ETH_TXD0

ETH_TXD1

ETH_TXD2

ETH_TXD3

ETH_TXCTL

ETH_RXCK

ETH_RXD0

ETH_RXD1

ETH_RXD2

ETH_RXD3

ETH_RXCTL

OTG_DATA4

OTG_DIR

OTG_STP

OTG_NXT

OTG_DATA0

OTG_DATA1

OTG_DATA2

OTG_DATA3

OTG_CLK

OTG_DATA5

OTG_DATA6

OTG_DATA7

SD_CMD

SD_D0

SD_D1

SD_D2

SD_D3

OTG_RESETN

SD_CD

UART_TX

UART_RX

ETH_MDC

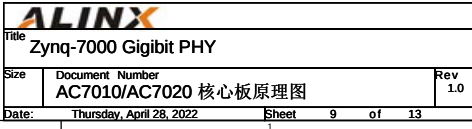
ETH_MDIO

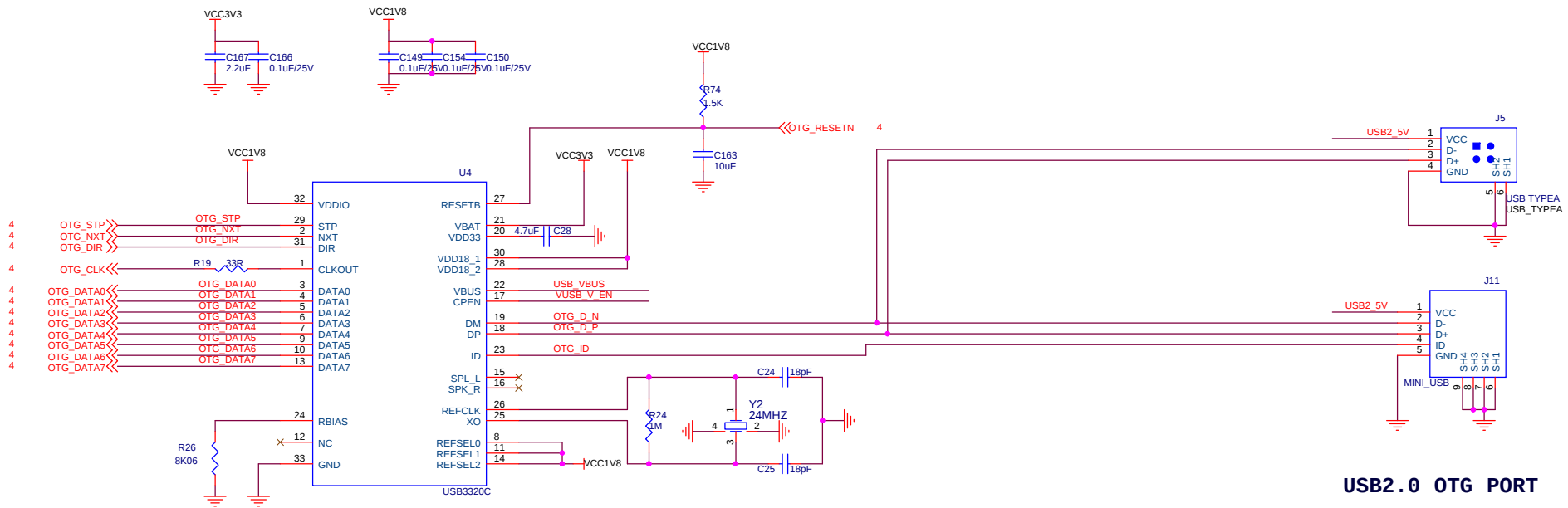
PS_SRST_B

R66 1K/1%

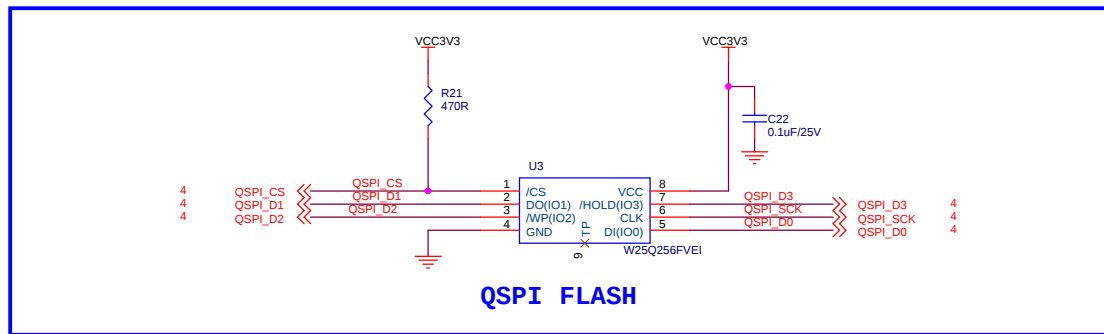
R65 1K/1%

C124 0.01uF

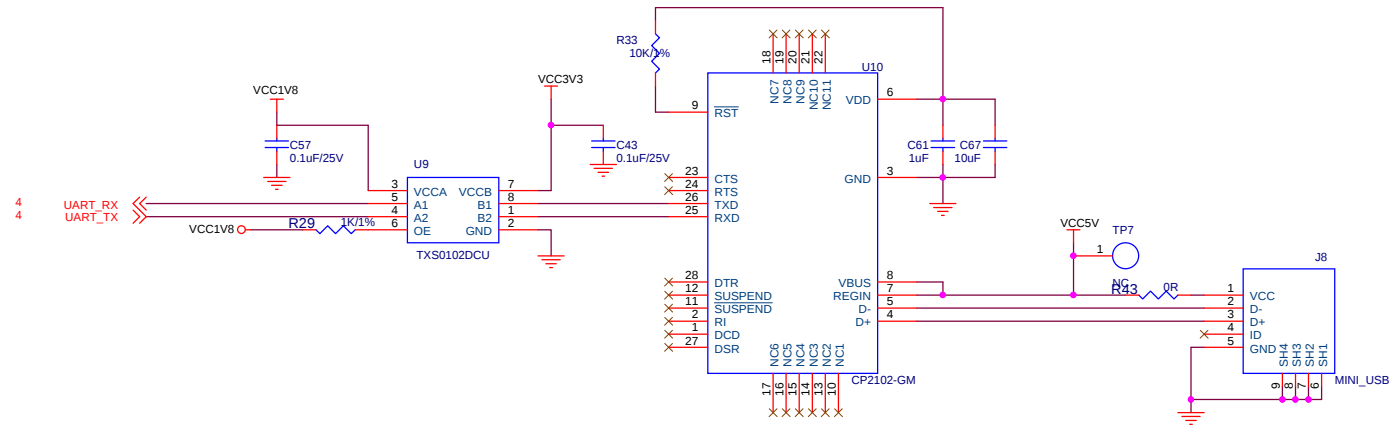




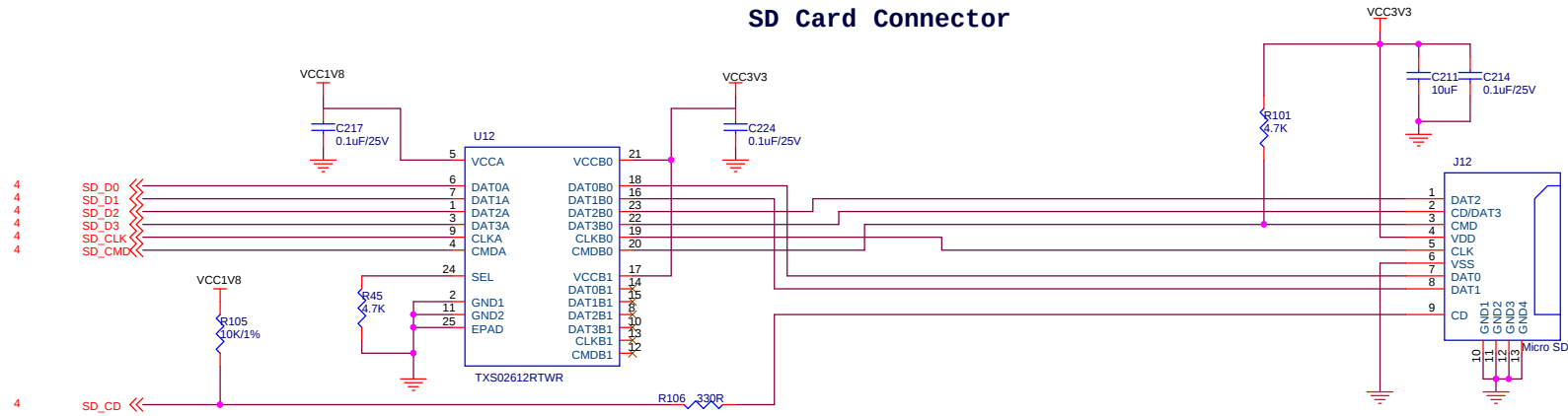
J5/J6 Connect: Host Mode
J5/J6 Not Connect: Slave/OTG Mode



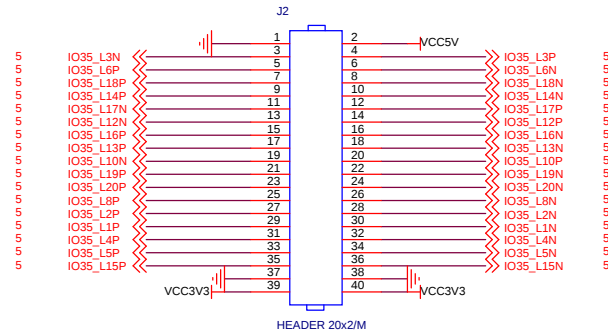
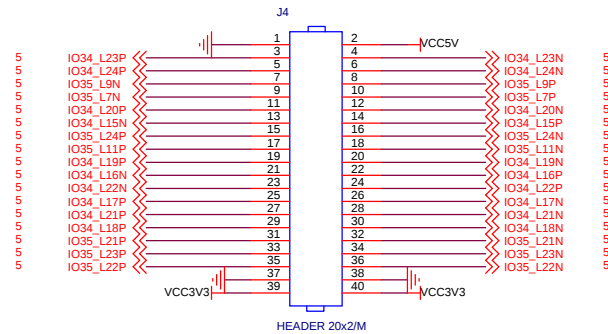
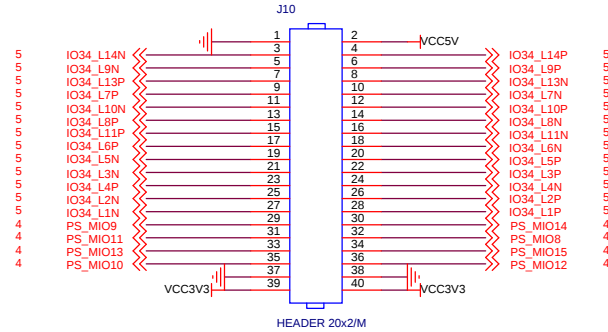
USB Uart

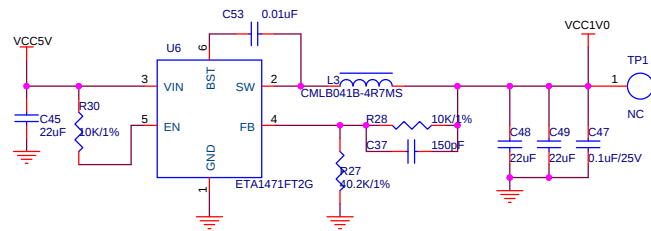


SD Card Connector

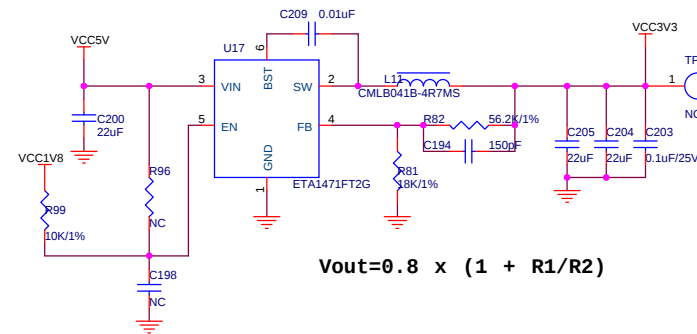


FPGA 40 PIN External IO

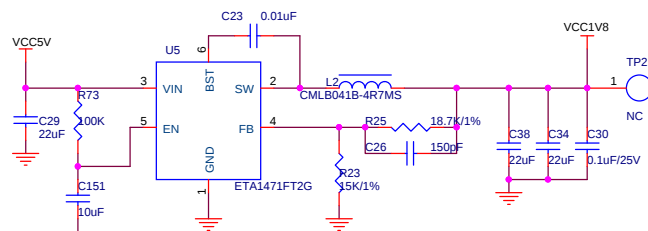




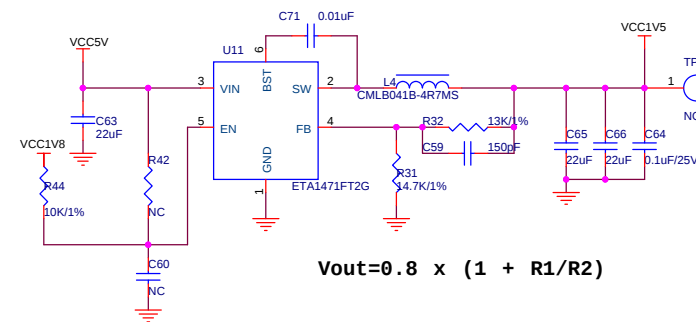
$$V_{out}=0.8 \times (1 + R1/R2)$$



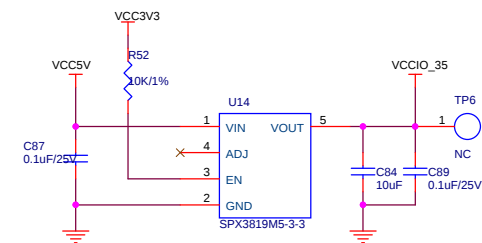
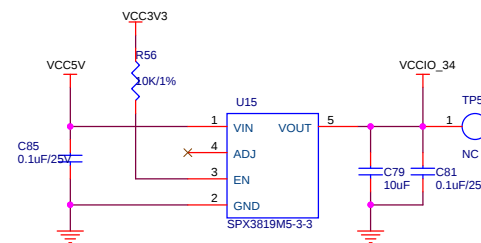
$$V_{out}=0.8 \times (1 + R1/R2)$$



$$V_{out}=0.8 \times (1 + R1/R2)$$



$$V_{out}=0.8 \times (1 + R1/R2)$$



Power On Sequence:

1.0V -> 1.8V -> 1.5 V -> 3.3V -> VCCIO